REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 and 10-13 are now in the applications. Claims 1, 2, 8, and 10 have been amended and claims 12 and 13 have been added. Claim 12 corresponds to the allowable claim 5 and claim 13 corresponds to the allowable claims 6 and 7 in combination. Claims 5, 6 and 7 have been retained in the original set of claims as well. In light of the indicated allowability of claims 5-7, claims 12 and 13 are in condition for allowance.

With reference to the drawing objection on page 2 of the Final Office action, enclosed herewith is a proposed flow chart, illustrating the primary steps of the method. Specifically, the flow chart mirrors the claimed invention as it is recited in claims 8, 10 and 11. Counsel has been careful not to introduce any new matter and to be guided only by the original disclosure when preparing the flow chart. If the proposed flow chart meets with the Examiner's approval, counsel will request formal entry of the drawing figure, including the necessary inserts in the specification.

It is regretfully noted that the Examiner once more rejected the claims of the instant application. As noted in the Interview Summary Record memorializing the interview of

January 18, 2005, as well as in the introduction to the detailed Office action, the Examiner had called to indicate that the claims would be allowed subject to minor changes. The changes have now been effected in claims 2 and 10. The suggested and requested change in the preamble of claim 8 has not been effected after having received the latest Office action and the corresponding rejection.

Claim 8, while having otherwise been amended, was not amended to change the preamble. The change is no longer warranted in view of the latest rejection over the reference Spix et al. We will return to this issue in the discussion of the differences between the claimed invention and the prior art of Spix.

More specifically, the Examiner had suggested to introduce claim 8 as "an error determination method" as opposed to the originally recited "in an error determination method." The difference, of course, is that claim 8 is an In re Dean claim, which is in effect a combination/subcombination claim. The differences between a simple combination claim and a combination/subcombination claim were highlighted in the last response and reference is made thereto. The difference is now even of greater importance in light of the new reference Spix et al.. The primary difference, however, is that the "scan paths" of Spix et al. have virtually nothing in common with

the "scan chains" of the instantly claimed method. Here, we have a program-controlled unit that uses scan chains with a plurality of elements. These same elements are the elements used in the program control unit itself. In other words, the program control unit processes a program, i.e. it is operated under program control, and when a certain pre-determined error is detected, the elements of the program control units are frozen and connected to scan chains and the scan chains then are read out.

We now turn to the art rejection, in which the claims have been rejected as being anticipated by Spix et al. (US 5,253,359) under 35 U.S.C. § 102(b).

The rejection is acknowledged. We further acknowledge that Spix et al., indeed, has disclosure, which appears to come quite close to the claimed invention. On further study, however, it is found that the similarities are purely coincidental and based on semantics. Spix et al. neither anticipates the invention nor renders it obvious. The primary issue with regard to Spix et al. is that the scan paths of the reference are entirely different from the scan chains according to the claimed invention.

The Examiner's specific referencing of column 3 in which Spix et al. disclose a maintenance architecture with integrated hardware and software for accessing and controlling internal machine registers is appreciated. We further make reference to column 8, which explains that the scan path logic performs various logic functions associated with scan paths. The statement in column 8, lines 17-20, explains the fact that the scan paths that are used by Spix et al. are provided for address decoding and serializing/deserializing. In other words, the scan path logic of Spix et al. would appear to be nothing but a gate array.

As explained in column 8, lines 40-45, when an error is detected in the clusters, then the scan path will have the error content contained therein and they may be read out to read the machine state information. As further explained, the information must be read out very quickly because otherwise the state of the scan path may be overwritten. This, of course, is quite different from the instantly claimed invention. Nevertheless, Spix et al. goes on toward the end of column 8 to explain that the single bit errors may not require a complete stoppage and freezing of the given cluster, but a double bit error may be fatal to system operation and it may require such freezing. In that case, the scan paths may latch the latest machine state and "halt the system clocks to

prevent overwrite of the error information". Col. 8, lines 65-68.

While this disclosure appears to come close to the claimed invention, it instead proves the distinction between the claimed invention and the prior art disclosure. There, the scan paths are transfer gates. They do not belong to the clusters and, in other words, they do not belong to the "plurality of elements" that change the logic state during program execution. When the system is stopped upon the detection of a given event, there is no such action as connecting the elements to scan chains and then to actually read out the scan chains and analyze the system. The scan paths of Spix et al. instead are transfer gates, which capture certain states of the clusters at certain clock periods. The registers are latched and, once they are frozen, there is no further reconnection of those latches of the register. In the instant case, of course, the elements of the program control unit are specifically connected to form scan chains and they are then read after they are connected to form the scan chains. Again, the claims are not directed to a transfer gate that serializes/deserializes the information coming out of the clusters. The scan path logic of the Spix et al. disclosure are connected scan paths and no suggestion is made towards

reconfiguring any of the scan paths, as in the instantly claimed invention.

Claim 8 has been further amended to clarify this further connection of the elements to form the scan chains. The insert is provided simply to clarify the claim further and it does not go beyond the original disclosure and the originally examined claims. Accordingly, the entry of the amendment to claim 8 is, respectfully, urged.

It is appreciated that the last action was made FINAL and that the last amendment made by applicants necessitated the new grounds of rejection. At the same time, it is respectfully urged, that the entry of the instantly proposed amendment does not move the claim content beyond the originally searched subject matter and it does not provide a new issue that requires further search and/or consideration. If anything, the added limitation in claim 8 further adapts on the method claim of the device of claim 1.

In summary, none of the prior art references, whether taken alone or in any combination, either show or suggest the features of claims 1-8, 12 and 13..These claims are, therefore, believed to be patentable over the art and since

all of the dependent claims are ultimately dependent thereon, they are allowable as well.

In view of the foregoing, reconsideration and allowance of claims 1-8 and 10-13 are solicited.

Attached please find payment in the amount of $200.00, reflecting charges for one additional independent claim.

Should any further objections remain, the Examiner is, respectfully, requested to telephone counsel, so that the matter may be resolved.

Respectfully submitted,

For Applicants

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